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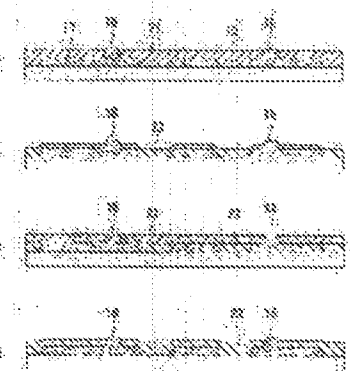
(54) MULTILAYER WIRING SUBSTRATE, MANUFACTURING METHOD OF MULTILAYER WIRING SUBSTRATE, ELECTRONIC DEVICE AND ELECTRONIC APPARATUS

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a multilayer wiring substrate, a manufacturing method of multilayer wiring substrates, an electronic device and an electronic apparatus, which can form elaborate multilayer wiring using a comparatively simple manufacture process.
SOLUTION: In the manufacturing method of a multilayer wiring substrate, which is constituted of a wiring layer of at least two layers (wiring patterns 17 and 31) and a polyimide (insulating film between layers) 22 and a conductive post between layers (conductive post) 18 that conducts between the wiring patterns 17 and 31, the polyimide 22 is provided around the conductive post between layers 18, using an entrainment discharge method.



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CLAIMS

[Claim(s)]
[Claim 1] the interlayer insulation film prepared between the two-layer wiring layer and this wiring layer at least, and the conductor which makes it flow through between these wiring layers -- the manufacture approach of a multilayer-interconnection substrate of coming to have a post -- it is -- said conductor -- the manufacture approach of the multilayer-interconnection substrate characterized by using a drop regurgitation method and preparing said interlayer insulation film around a post.
[Claim 2] Said interlayer insulation film is the manufacture approach of the multilayer-interconnection substrate according to claim 1 characterized by forming using the liquid of hypoviscosity.
[Claim 3] said conductor -- the manufacture approach of the multilayer-interconnection substrate according to claim 1 or 2 characterized by forming a post by the drop regurgitation method.
[Claim 4] The manufacture approach of claim 1 characterized by forming wiring about at least one wiring layer in said wiring layer by the drop regurgitation method thru/or the multilayer-interconnection substrate of three given in any 1 term.
[Claim 5] said interlayer insulation film, said wiring layer, and said conductor -- the manufacture approach of the multilayer-interconnection substrate according to claim 1 characterized by forming all the posts by the drop regurgitation method.
[Claim 6] said interlayer insulation film, said wiring layer, and said conductor -- the manufacture approach of the multilayer-interconnection substrate according to claim 1 characterized by forming all the posts using the same drop regurgitation equipment.
[Claim 7] said wiring and a conductor -- the manufacture approach of claim 3 characterized by formation of a post having the process which repeats by turns the regurgitation to the substrate of conductive ink, and desiccation of this conductive ink by which the regurgitation was carried out thru/or the multilayer-interconnection substrate of six given in any 1 term.
[Claim 8] The manufacture approach of claim 1 characterized by giving a water-repellent finish in the regurgitation-ed side of this substrate before carrying out the regurgitation of the drop to a substrate by said drop regurgitation method thru/or the multilayer-interconnection substrate of seven given in any 1 term.
[Claim 9] The manufacture approach of claim 1 characterized by forming an acceptance layer in the regurgitation-ed side of this substrate before making the regurgitation a subetrate by said drop regurgitation method thru/or the multilayer-interconnection substrate of seven given in any 1 term.
[Claim 10] said wiring and a conductor -- the manufacture approach of claim 1 which has and forms the process which calcinates the conductive ink which the post was breathed out by the substrate and dried thru/or the multilayer-interconnection substrate of nine given in any 1 term.
[Claim 11] Formation of said interlayer insulation film is the manufacture approach of claim 1 characterized by having the process which carries out the regurgitation of the liquid containing polyimide or a polyimide precursor to a subetrate thru/or the multilayer-interconnection substrate of ten given in any 1 term.
[Claim 12] Formation of said interlayer insulation film is the manufacture approach of the multilayer-interconnection substrate according to claim 11 characterized by having the process which calcinates

this substrate after the process which carries out the regurgitation of the liquid containing said polyimide or a polyimide precursor to a substrate.
[Claim 13] the height of said interlayer insulation film -- said conductor -- the height of a post, and abbreviation -- the manufacture approach of the multilayer-interconnection substrate according to claim 10 characterized by adjusting the amount of the drop breathed out by said drop regurgitation method, the consistency which arranges this drop, and the count of a regurgitation scan so that it may become the same.
[Claim 14] the height of said interlayer insulation film -- said conductor -- the height of a post, and abbreviation -- it becomes the same -- as -- this interlayer insulation film -- and -- this -- a conductor -- a post -- forming -- this interlayer insulation film -- or -- this -- a conductor -- a post top -- the manufacture approach of claim 1 thru/or the multilayer-interconnection substrate of 13 given in any 1 term -- using -- said wiring layer, said layer insulation layer, and said conductor -- the manufacture approach of the multilayer-interconnection substrate characterized by forming at least one of posts.
[Claim 15] The manufacture approach of the multilayer-interconnection substrate characterized by using the manufacture approach of claim 1 thru/or the multilayer-interconnection substrate of 14 given in any 1 term for the chip which has an integrated circuit, and forming a multilayer interconnection.
[Claim 16] approaches other than the manufacture approach of 14 claim 1 thru/or given in any 1 term -- a wiring layer, an interlayer insulation film, and a conductor -- the manufacture approach of the multilayer-interconnection substrate characterized by using the manufacture approach of 14 claim 1 thru/or given in any 1 term to the substrate with which at least one of posts was formed.
[Claim 17] the interlayer insulation film prepared between the two-layer wiring layer and this wiring layer at least, and the conductor which makes it flow through between these wiring layers -- the multilayer-interconnection substrate which comes to have a post -- it is -- said wiring layer, an interlayer insulation film, and a conductor -- the multilayer-interconnection substrate with which at least one of posts is characterized by being manufactured by the manufacture approach of claim 1 thru/or the multilayer-interconnection substrate of 16 given in any 1 term.
[Claim 18] the interlayer insulation film prepared between the two-layer wiring layer and this wiring layer at least, and the conductor which makes it flow through between these wiring layers -- the multilayer-interconnection substrate which comes to have a post -- it is -- said conductor -- the multilayer-interconnection substrate characterized by for thickness being 20 micrometers from 1 micrometer, and a post being the configuration on which the diameter turned down the 10 to 200 micrometers bowl.
[Claim 19] the height of said interlayer insulation film, and said conductor -- the height of a post -- abbreviation -- the multilayer-interconnection substrate according to claim 18 characterized by the same thing.
[Claim 20] The multilayer-interconnection substrate according to claim 18 or 19 characterized by forming the top face of said interlayer insulation film in an abbreviation flat surface.
[Claim 21] a wiring layer, the interlayer insulation film prepared on this wiring layer, and the conductor prepared so that it may pierce through said interlayer insulation film, while connecting with wiring of said wiring layer -- the electron device which comes to have a post -- it is -- said wiring layer, an interlayer insulation film, and a conductor -- the electron device with which at least one of posts is characterized by being manufactured by the manufacture approach of 16 claim 1 thru/or given in any 1 term.
[Claim 22] a wiring layer, the interlayer insulation film prepared on this wiring layer, and the conductor prepared so that it may pierce through said interlayer insulation film, while connecting with wiring of said wiring layer -- the electron device which comes to have a post -- it is -- said conductor -- the electron device characterized by for thickness being 20 micrometers from 1 micrometer, and a post being the configuration on which the diameter turned down the 10 to 200 micrometers bowl.
[Claim 23] the height of said interlayer insulation film, and said conductor -- the height of a post -- abbreviation -- the electron device according to claim 22 characterized by the same thing.

[Claim 24] The electron device according to claim 22 or 23 characterized by forming the top face of said interlayer insulation film in an abbreviation flat surface.
[Claim 25] Electronic equipment characterized by having claim 17 thru/or the multilayer-interconnection substrate of 20 given in any 1 term.
[Claim 26] Electronic equipment characterized by having the electron device of 24 claim 21 thru/or given in any 1 term.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of a multilayer-interconnection substrate and a multilayer-interconnection substrate, an electron device, and electronic equipment.
[0002]
[Description of the Prior Art] There are some which are conventionally depended on the following process as an approach of manufacturing a multilayer printed-circuit board. First, alignment of the monolayer substrate which carried out pattern formation by etching is carried out, and the laminating of each class is carried out. Subsequently, a through hole is made in the position of a substrate in order to connect an up-and-down wiring layer electrically. And the multilayer printed-circuit board was formed by giving a flow by plating etc. or filling the perimeter of the through hole with a conductive paste. However, since the pad for element placements was not able to be formed in the part of a through hole, and since the diameter of a through hole was also usually about 0.3mm, such an approach was difficult for using for high density assembly.
[0003] In recent years, in order to raise a surface mount consistency more, the method which takes the electrical installation between layers by the non-penetrating interlayer connection (it is called "IVH" an interstitial beer hall and the following) is used. The resin multilayer printed wiring board which can carry out the interlayer connection of all the layers in IVH is put in practical use by carrying out metal plating of the non-through hole prepared in the insulating layer by it using the photopolymer or it filled the open beam hole with the conductive paste to the insulating layer by using such a method etc.
[0004] However, all once made the hole in the insulating layer, and have taken how to make the interior of the hole into conductivity with plating or a conductive paste, and the above-mentioned conventional approach had the trouble that a production process became complicated.
[0005] on the other hand — JP,6-57455,B — an insulating layer — a hole — not opening — a lower layer wiring top — a photolithography — using — the conductor previously for interlayer connections — a post — forming — subsequently — a conductor — the perimeter of a post — resin — applying — a

hotpress -- a conductor -- the approach of forming a multilayer interconnection is indicated by forming an insulator layer so that a posttop face may be exposed, and subsequently forming the upper wiring. moreover, the object for interlayer connections above-mentioned in JP,9-46045,A -- a conductor -- the approach of forming a post by deposition of a stud bump, a conductive ball, and a metal particle is indicated.

[0006]

[Problem(s) to be Solved by the Invention] however -- the approach currently indicated by the above-mentioned official report -- lower layer wiring and the conductor for interlayer connections -- since a post is formed by the option, a production process becomes complicated. after [moreover,] applying an insulator layer to the whole surface by the approach currently indicated by the above-mentioned official report -- a hotpress -- a conductor -- since the top face of a post is exposed -- a conductor -- there was a trouble that the height of a post needed to arrange thoroughly.

[0007] Moreover, when JP,2000-204479,A also draws and carries out stoving of the solution of an insulator by the desired pattern, without vacating a hole for an insulating layer, the approach of forming an insulator layer selectively is indicated. Moreover, by the approach currently indicated by JP,2000-204479,A, about the conductor pattern, the activator for electroless deposition, such as a silane coupling agent, is selectively applied by a drop regurgitation method (ink jet method) etc., and the circuit pattern is selectively formed by plating after that. Thus, three dimensions wiring structure can be formed by carrying out pattern spreading so that an insulating layer and a conductor layer may be formed in predetermined sequence.

[0008] however, since the plating process is used, the trouble that it is difficult to form an elaborate pattern [as / whose width of face of a line/tooth space is 20 micrometers / 20 micrometers], and waste fluid processing are required of the above-mentioned Prior art -- etc. -- there was a trouble.

[0009] This invention aims at offer of the manufacture approach of the multilayer-interconnection substrate which makes it possible to form an elaborate multilayer interconnection by the comparatively simple production process, and a multilayer-interconnection substrate, an electron device, and electronic equipment.

[0010]

[Means for Solving the Problem] the interlayer insulation film with which the manufacture approach of the multilayer-interconnection substrate of this invention was established between the two-layer wiring layer and this wiring layer at least in order to attain the above-mentioned object, and the conductor which makes it flow through between these wiring layers -- the manufacture approach of a multilayer-interconnection substrate of coming to have a post -- it is -- said conductor -- it is characterized by using a drop regurgitation method and preparing said interlayer insulation film around a post. According to such an approach, when forming an interlayer insulation film, since a photolithography, etching, and a drilling process become unnecessary, the production process of a multilayer-interconnection substrate can be made simple, and the miniaturization of a manufacturing installation, shortening of a manufacture period, and reduction-ization of a manufacturing cost are attained. Moreover, according to such an approach, when forming an interlayer insulation film, since a mask becomes unnecessary, for example, it becomes possible from CAD data to form a direct interlayer insulation film, the period from a design to completion is shortened, and it can respond also to a design change easily. moreover -- since an interlayer insulation film is prepared by the drop regurgitation method according to such an approach -- a conductor -- the top face of a post can form an interlayer insulation film in the condition of having exposed certainly.

[0011] Moreover, as for the manufacture approach of the multilayer-interconnection substrate of this invention, it is desirable that said interlayer insulation film is formed using the liquid of hypoviscosity. the conductor which according to such an approach is formed after the lower layer wiring of the self-leveling effectiveness even if some level differences are in lower layer wiring -- it becomes the flat field which had the top face of a post, and complete set of top face of an interlayer insulation film, and the

multilayer-interconnection substrate of good structure can be formed.
[0012] moreover, the manufacture approach of the multilayer-interconnection substrate of this invention -- said conductor -- it is desirable to form a post by the drop regurgitation method. according to such an approach -- a conductor -- when forming a post, since a photolithography, etching, and a drilling process become unnecessary, the production process of a multilayer-interconnection substrate can be made simple, and the miniaturization of a manufacturing installation, shortening of a manufacture period, and reduction-ization of a manufacturing cost are attained. moreover -- according to such an approach -- a conductor -- direct [from CAD data], for example, since a mask becomes unnecessary, when forming a post -- a conductor -- it becomes possible to form a post, the period from a design to completion is shortened, and it can respond now also to a design change easily.
[0013] Moreover, as for the manufacture approach of the multilayer-interconnection substrate of this invention, it is desirable to form wiring about at least one wiring layer in said wiring layer by the drop regurgitation method. According to such an approach, when forming wiring, since a photolithography, etching, and a drilling process become unnecessary, the production process of a multilayer-interconnection substrate can be made simple, and the miniaturization of a manufacturing installation, shortening of a manufacture period, and reduction-ization of a manufacturing cost are attained moreover, direct [from CAD data], for example according to such an approach, since a mask becomes unnecessary, when forming wiring -- a conductor -- it becomes possible to form a post, the period from a design to completion is shortened, and it can respond now also to a design change easily
[0014] moreover, the manufacture approach of the multilayer-interconnection substrate of this invention -- said interlayer insulation film, said wiring layer, and said conductor -- it is desirable to form all the posts by the drop regurgitation method. According to such an approach, since a photolithography, etching, and a drilling process become unnecessary about all the processes of a multilayer-interconnection substrate, the production process of a multilayer-interconnection substrate can be made substantially simple, and the miniaturization of the further manufacturing installation, shortening of a manufacture period, and reduction-ization of a manufacturing cost are attained. Moreover, according to such an approach, since a mask becomes unnecessary about all the processes of a multilayer-interconnection substrate, for example, it becomes possible from CAD data to form a direct multilayer-interconnection substrate, the period from a design to completion is shortened more, and it can respond also to a design change easily.
[0015] moreover, the manufacture approach of the multilayer-interconnection substrate of this invention -- said interlayer insulation film, said wiring layer, and said conductor -- it is desirable to form all the posts using the same drop regurgitation equipment. According to such an approach, drop regurgitation equipment has two or more discharge heads, or if it is the head of structure which supplies two or more liquids (ink) to two or more nozzle groups of one head independently like the color ink jet printer for the usual image printing Only by replacing the electronic file (bit map) which controls a spreading pattern one drop regurgitation equipment -- an interlayer insulation film, a wiring layer, and a conductor -- since a post can be formed, shortening of the further manufacture period and reduction-ization of a manufacturing cost are attained, and it can respond also to a design change still more easily.
[0016] moreover, the manufacture approach of the multilayer-interconnection substrate of this invention -- said wiring and a conductor -- as for formation of a post, it is desirable to have the process which repeats by turns the regurgitation to the substrate of conductive ink and desiccation of this conductive ink by which the regurgitation was carried out. repeating the regurgitation of the conductive ink to a substrate, and desiccation by turns according to such an approach -- wiring or a conductor -- thickness of the electric conduction film to post can be enlarged gradually, and it can be made desired thickness and desired height. Moreover, since liquid repellance is to the conductive ink which contains the same metal particle in that spreading film after drying the conductive ink (solvent) containing a metal particle by this approach, it is effective in the ability to earn only the thickness of the height direction, without spreading, even if it applies conductive ink to that spreading film in piles. then,

this effectiveness -- using -- a required part -- a conductor -- a post can be formed.
[0017] Moreover, before the manufacture approach of the multilayer-interconnection substrate of this invention carries out the regurgitation of the drop to a substrate by said drop regurgitation method, it is desirable to give a water-repellent finish in the regurgitation-ed side of this substrate. According to such an approach, width of face of wiring can be narrowed and more precise wiring structure can be formed.
[0018] Moreover, before the manufacture approach of the multilayer-interconnection substrate of this invention makes the regurgitation a substrate by said drop regurgitation method, it is desirable to form an acceptance layer in the regurgitation-ed side of this substrate. according to such an approach -- a position -- wiring and a conductor -- it becomes easy to form a post.
[0019] moreover, the manufacture approach of the multilayer-interconnection substrate of this invention -- said wiring and a conductor -- it is desirable to have and form the process which calcinates the conductive ink which the post was breathed out by the substrate and dried. According to such an approach, electric conductivity can be made to discover in the conductive ink breathed out by the substrate. That is, since electric conductivity is not discovered only by drying conductive ink, electric conductivity is made to discover by calcinating.
[0020] Moreover, as for the manufacture approach of the multilayer-interconnection substrate of this invention, it is desirable to have the process which carries out the regurgitation of the liquid with which formation of said interlayer insulation film contains polyimide or a polyimide precursor to a substrate. According to such an approach, after carrying out and carrying out the drop regurgitation to the viscosity which can dilute and carry out the drop regurgitation of the precursor of polyimide with a solvent for example, an interlayer insulation film can be formed by calcinating by 300-degree Centigrade.
[0021] Moreover, as for the manufacture approach of the multilayer-interconnection substrate of this invention, it is desirable to have the process which calcinatex this substrate after the process to which formation of said interlayer insulation film carries out the regurgitation of the liquid containing said polyimide or a polyimide precursor to a substrate.
[0022] moreover, the manufacture approach of the multilayer-interconnection substrate of this invention -- the height of said interlayer insulation film -- said conductor -- the height of a post, and abbreviation -- it is desirable to adjust the amount of the drop breathed out by said drop regurgitation method, the consistency which arranges this drop, and the count of a regurgitation scan so that it may become the same, according to such an approach -- the height (thickness) of an interlayer insulation film, and a conductor -- the height (thickness) of a post -- abbreviation -- the multilayer-interconnection substrate of the good structure which becomes the same can be formed. moreover -- the case where the self-leveling effectiveness is expectable in carrying out pattern spreading by the drop regurgitation method according to such an approach -- a conductor -- spreading for forming an interlayer insulation film (a conductor -- the part of a post -- avoiding), using the negative pattern of a bit map used for forming a post as it is can be performed. the conductor after performing spreading for forming an interlayer insulation film on the other hand until it becomes the same height as lower layer wiring so that lower layer wiring may once be avoided, when the self-leveling effectiveness can seldom expect -- same spreading is performed so that the part of a post may be avoided. And it can calcinate at the end and the interlayer insulation film which consists of polyimide etc. can be completed.
[0023] moreover, the manufacture approach of the multilayer-interconnection substrate of this invention -- the height of said interlayer insulation film -- said conductor -- the height of a post, and abbreviation -- it becomes the same -- as -- this interlayer insulation film -- and -- this -- a conductor -- a post -- forming -- this interlayer insulation film -- or -- this -- a conductor -- a post top -- the manufacture approach of claim 1 thru/or the multilayer-interconnection substrate of 13 given in any 1 term -- using -- said wiring layer, said layer insulation layer, and said conductor -- it is characterized by forming at least one of posts. According to such an approach, a multilayer-interconnection substrate can be manufactured by the simple production process, namely, a conductor -

- the top face of a post -- exposing -- the other part -- a conductor -- after being in the condition of having been covered with the interlayer insulation film of the same height as a posttop face, the multilayer interconnection which does not have a limit about a number of layers theoretically can be again formed by repeating a water-repellent finish of a substrate, wiring formation with a drop regurgitation method and electric conduction post formation, baking, formation of an interlayer insulation film, baking, etc. the number of predetermined times.

[0024] Moreover, the manufacture approach of the multilayer-interconnection substrate of this invention is characterized by using the manufacture approach of claim 1 thru/or the multilayer-interconnection substrate of 14 given in any 1 term for the chip which has an integrated circuit, and forming a multilayer interconnection. According to such an approach, a multilayer interconnection can be suddenly formed by the drop regurgitation on IC (integrated circuit) chip.

[0025] moreover, the manufacture approach of the multilayer-interconnection substrate of this invention -- approaches other than the manufacture approach of 14 claim 1 thru/or given in any 1 term -- it is -- a wiring layer, an interlayer insulation film, and a conductor -- it is characterized by using the manufacture approach of 14 claim 1 thru/or given in any 1 term to the substrate with which at least one of posts was formed. According to such an approach, a multilayer interconnection can be formed to the substrate formed to the middle using the manufacture approach of the multilayer-interconnection substrate of this invention by the manufacture approach other than the manufacture approach of the multilayer-interconnection substrate of this invention. This approach is suitable to correspond to for example, double-sided mounting. for example, before [after forming a pattern in the substrate of an innermost layer] that -- a through hole -- opening -- it -- a metal paste etc. -- burying -- after that -- a conductor -- the multilayer-interconnection substrate mounted in both sides by using the manufacture approach of this invention from the process which stands a post can be formed only using a drop regurgitation method.

[0026] moreover, the interlayer insulation film with which the multilayer-interconnection substrate of this invention was formed between the two-layer wiring layer and this wiring layer at least and the conductor which makes it flow through between these wiring layers -- the multilayer-interconnection substrate which comes to have a post -- it is -- said wiring layer, an interlayer insulation film, and a conductor -- at least one of posts is characterized by being manufactured by the manufacture approach of claim 1 thru/or the multilayer-interconnection substrate of 18 given in any 1 term. according to such a substrate -- said wiring layer, an interlayer insulation film, or a conductor -- when forming a post, since a drop regurgitation method is used, a high-density multilayer interconnection can be formed in high degree of accuracy.

[0027] moreover, the interlayer insulation film with which the multilayer-interconnection substrate of this invention was formed between the two-layer wiring layer and this wiring layer at least and the conductor which makes it flow through between these wiring layers -- the multilayer-interconnection substrate which comes to have a post -- it is -- said conductor -- thickness is 20 micrometers from 1 micrometer, and a post is characterized by being the configuration on which the diameter turned down the 10 to 200 micrometers bowl. according to such a substrate -- a conductor -- since the post is minute, a high-dehsity multilayer interconnection can be formed in high degree of accuracy.

[0028] moreover, the multilayer-interconnection substrate of this invention -- the height of said interlayer insulation film, and said conductor -- the height of a post -- abbreviation -- the same thing is desirable. According to such a substrate, a multilayer-interconnection substrate with many number of layerses can be formed easily.

[0029] Moreover, as for the multilayer-interconnection substrate of this invention, it is desirable that the top face of said interlayer insulation film is formed in an abbreviation flat surface. According to such a substrate, a multilayer-interconnection substrate with many number of layerses can be formed in high degree of accuracy.

[0030] moreover, the conductor prepared so that it may pierce through said interlayer insulation film,

while the electron device of this invention is connected to a wiring layer, the interlayer insulation film prepared on this wiring layer, and wiring of said wiring layer -- the electron device which comes to have a post -- it is -- said wiring layer, an interlayer insulation film, and a conductor -- at least one of posts is characterized by being manufactured by the manufacture approach of 16 claim 1 thru/or given in any 1 term. According to such an electron device, a high-density multilayer interconnection can be formed in high degree of accuracy.

[0031] moreover, the conductor prepared so that it may pierce through said interlayer insulation film, while the electron device of this invention is connected to a wiring layer, the interlayer insulation film prepared on this wiring layer, and wiring of said wiring layer -- the electron device which comes to have a post -- it is -- said conductor -- thickness is 20 micrometers from 1 micrometer, and a post is characterized by being the configuration on which the diameter turned down the 10 to 200 micrometers bowl. according to such an electron device -- a conductor -- since the post is minute, the electron device of a minute configuration can be constituted and an electronic instrument can be miniaturized.

[0032] moreover, the electron device of this invention -- the height of said interlayer insulation film, and said conductor -- the height of a post -- abbreviation -- the same thing is desirable. According to such an electron device, an electron device with many number of layerses can be formed in high degree of accuracy, and an electronic instrument can be miniaturized.

[0033] Moreover, as for the electron device of this invention, it is desirable that the top face of said interlayer insulation film is formed in an abbreviation flat surface. According to such an electron device, an electron device with many number of layerses can be formed in high degree of accuracy, and a miniaturization and elaboration of an electronic instrument become possible.

[0034] Moreover, the electronic equipment of this invention is characterized by having said multilayer-interconnection substrate. According to this invention, it becomes possible to carry out reduction-izing and a miniaturization of a manufacturing cost, shortening the production time of electronic equipment.

[0035] Moreover, the electronic equipment of this invention is characterized by having said electron device. According to this invention, it becomes possible to carry out reduction-izing and a miniaturization of a manufacturing cost, shortening the production time of electronic equipment.

[0036]

[Embodiment of the Invention] Hereafter, the manufacture approach of the multilayer-interconnection substrate concerning this invention is explained based on a drawing.

(The 1st operation gestalt) Drawing 1 thru/or drawing 3 are process drawings showing the manufacture approach of the multilayer-interconnection substrate concerning the 1st operation gestalt of this invention. Drawing 1 shows from ** ink down stream processing to layer post formation. Drawing 2 shows the interlayer insulation film formation process. Drawing 3 shows the process after bilayer eye circuit pattern formation. Multilayer printed wiring is formed in the one side side of a substrate 10 with this operation gestalt.

[0037] <Conductive ink> First, it is the liquid breathed out from drop regurgitation equipment, and the conductive ink used when forming multilayer printed wiring is explained. With this operation gestalt, the golden particle dispersion liquid (vacuum metallurgy company make, trade name "perfect gold") which distributed the golden particle with a diameter of about 10nm in toluene are diluted with toluene, it adjusts so that that viscosity may be set to 3 [mPa-s], and this liquid is used as conductive ink.

[0038] The ** ink processing (water-repellent finish) performed to <** ink down stream processing>, next the front face of a substrate is explained. By performing this ** ink processing, the location of the conductive ink breathed out on the substrate is more controllable to high degree of accuracy. First, the substrate 10 which consists of polyimide is irradiated in IPA, ultraviolet rays with an after [washing] and a wavelength of 254nm are irradiated for 10 minutes by the reinforcement of 10 mW/cm2, and it washes further (UV irradiation washing). In order to perform ** ink processing to this substrate 10, the hexa deca fluoroes 1, 1, 2, and 2, and tetrahydro decyltriethoxysilane 0.1g and a substrate 10 are put into a well-closed container with a volume of 10l., and it holds by 120-degree Centigrade for 2 hours.

Thereby, the monomolecular film of ** ink nature is formed on a substrate 10. The contact angle of the front face of a substrate 10 in which this monomolecular film was formed, and the above-mentioned conductive ink by which the drop was carried out on that front face becomes about 70 degrees.

[0039] The contact angle of the substrate front face after the above-mentioned ** ink processing and conductive ink is too large in order to form multilayer printed wiring by the drop regurgitation method. Then, the ultraviolet rays of the same wavelength (254nm) as the time of carrying out said washing to this substrate 10 are irradiated for 2 minutes. Consequently, the contact angle on conductive ink and the front face of a substrate becomes about 35 degrees. In addition, an acceptance layer may be formed instead of ** ink processing.

[0040] The regurgitation of the above-mentioned conductive ink is carried out to the substrate 10 with which the <1st layer wiring formation process> ****** ink processing was performed. This is breathed out as a drop 12 from the ink jet head 11 of drop regurgitation equipment, and it is performed so that it may become the bit map pattern of a predetermined dot space. Subsequently, it heat-treats and an electric conduction film pattern is formed.

[0041] Here, as an ink jet head 11, the head of a commercial printer (trade name "PM950C") is used, for example. Moreover, since the ink inhalation section is a product made from plastics, what changed the inhalation section into the metal fixture so that it might not dissolve to an organic solvent is used. If the regurgitation of the above-mentioned conductive ink is carried out using driver voltage of the ink jet head 11 as 20V, the drop 12 of the volume of a 6pico liter will be breathed out. The diameter of the drop 12 is about 27 micrometers. After a drop 12 reaches the target on a substrate 10 (35 contact angles), the drop 12 spreads in diameter of about 45 micrometers on a substrate 10.

[0042] As a circuit pattern which draws on a substrate 10, on the grid which consists of a square which is 50 micrometers, one side designed as a monochrome binary bit map, and formed by carrying out the regurgitation of the drop 12 according to this bit map, for example. That is, as shown in drawing 1 (a), the conductive ink which contains a golden particle on a substrate 10 from the ink jet head 11 was breathed out so that it might become the arrangement in every 50 micrometers.

[0043] Since one drop 13 which reached the substrate 10 spreads in diameter of about 45 micrometers on condition that the above, drop 13 adjacent comrades did not contact but all dots (drop 13) are isolated on a substrate 10. It once cooled naturally for several minutes after performing the pattern regurgitation until it hit the hot blast of 100-degree Centigrade to the substrate 10 for 15 seconds and the substrate 10 returned to the room temperature after that, in order to dry the solvent of conductive ink. Consequently, it will be in the condition which shows in drawing 1 (b).

[0044] After this processing, the ** ink nature of a substrate 10 is not different from before processing. Moreover, the thickness of the ink droplet 14 which the solvent was flown from the drop 13 by desiccation etc., and was formed is set to about 2 micrometers. Moreover, the ** ink nature on this ink droplet 14 turns into ** ink nature almost comparable as a part without an ink droplet 14.

[0045] Then, the regurgitation of the drop 15 which aims at the medium of a dot (ink droplet 14) when the **** was isolated like drawing 1 (c), and consists of the same liquid as a drop 13 on the same conditions as the above again is carried out. In drawing 1 , although only the sectional view is shown, when the same isolated dot as an ink droplet 14 exists also in this Fig. (space) and a perpendicular direction, the medium of the dot breathes out the drop 15 similarly. By this regurgitation, the almost same result as the case of the regurgitation to a substrate 10 and the substrate 10 which does not have an ink droplet 14 at the regurgitation in the above-mentioned conditions since the liquid repellance on an ink droplet 14 was almost the same is obtained.

[0046] Then, hot air drying is performed like [drop / 15] the above, the solvent of conductive ink is volatilized, and the pattern 16 with which all the ink droplets were connected is formed like drawing 1 (d) of this. Furthermore, in order to earn thickness, and in order to make it the configuration of a dot not remain in a circuit pattern, the line breadth of 50 micrometers and the circuit pattern 17 of 10 micrometers of thickness as show the regurgitation which aims at the medium of the dot performed like

the above, and the course of hot air drying repeatedly to drawing 1 (e) also including a part as stated above a total of 6 times are formed. In addition, only by flying the solvent of conductive ink in this phase, since baking is inadequate, there is no electrical conductivity in a circuit pattern.

[0047] The layer flow post (conductor post) 18 for penetrating a <layer flow post formation process>, next an interlayer insulation film, and aiming at a flow with a bilayer eye which it is is formed. Here, a layer flow post can be formed at the completely same process as the above-mentioned 1st layer wiring formation process. That is, the flow between layers carries out the regurgitation of the conductive ink which contained the silver particle only in the required location in piles on both sides of hot air drying discharge and in between. And as a total of 6 times of regurgitation shows to drawing 1 (f), the height from an eye forms further the layer flow post 18 which is 10 micrometers.

[0048] Then, the substrate 10 by which pattern formation was carried out is heat-treated for 30 minutes by 300-degree Centigrade in atmospheric air, and silver particles are contacted electrically. Thereby, it is formed in the form which the circuit pattern 17 of the 1st layer and the layer flow post 18 unified. Moreover, the thickness of a circuit pattern 17 and the layer flow post 18 whole serves as the abbreviation half before heat treatment like drawing 1 (g) by this heat treatment. Here, the electrical conductivity of a silver circuit pattern is set to about 2 [muomegacm]. When assessment according the adhesion force of a circuit pattern 17 and a substrate 10 to a Scotch tape (trademark) trial is performed, it turns out that there is no peeling and there is sufficient adhesion force.

[0049] In forming a <interlayer insulation film formation process>, next an interlayer insulation film, ultraviolet rays with a wavelength of 256nm were irradiated for 5 minutes by the reinforcement of 10 [mW/cm2] as pretreatment at the substrate 10 with which the circuit pattern 17 of an eye was formed further, this -- the front face of a substrate 10 -- and the circuit pattern 17 top of an eye serves as parent ink nature further.

[0050] As ink 21 for forming an interlayer insulation film, the commercial polyimide varnish (the Du Pont make, product name "Pile ML") was diluted with the solvent (N-methyl-2-pyrrolidone), and it adjusted and used, for example so that viscosity might be set to 20 [mPa-s]. It applied so that the part of the layer electric conduction post 18 might be avoided with the same equipment as the drop regurgitation equipment which used this ink 21 by formation of the conductive pattern in the above-mentioned 1st layer wiring formation process. Although the amount of an ink droplet is made for example, into a 5pico liter, after reaching substrate 10 front face and circuit pattern 17 of parent ink nature, it wets wet and spreads, and all parts other than the layer electric conduction post section are covered in ink 21. Moreover, the front face of ink 21 becomes flat according to the self-leveling effectiveness. And as drawing 2 (a) shows, the layer electric conduction post 18 gives two coats of ink 21 several times with drop regurgitation equipment to the height which comes out from the oil level of ink 21 slightly (about 0.1 micrometers).

[0051] Subsequently, this subetrate 10 was heat-treated for 30 minutes by 400-degree Centigrade, and clearance of a solvent and hardening of polyimide were performed. Consequently, as shown in drawing 2 (b), the thickness of polyimide 22 serves as the abbreviation half of the ink 21 before heat treatment. Then, pattern spreading of the ink 21 is carried out on polyimide 22 like the above once again, and as shown in drawing 2 (c), the layer electric conduction post 18 comes out from the oil level of ink 21 slightly. And if it heat-treats for 30 minutes and is made to harden by 400-degree Centigrade like the above, as shown in drawing 2 (d), the thickness of polyimide 22 will be set to a total of 8 micrometers in the thinnest part.

[0052] In this condition, the irregularity which reflected the circuit pattern of an eye further is seen in the front face of polyimide 22. However, if the process (it applies and calcinates to height until a posttop face comes out slightly) same once again as the above is performed, it will approach still more evenly. Moreover, it is the same, even if it does not apply a polyimide precursor to the whole surface, but it applies only to a crevice and it calcinates.

[0053] By repeating such a process several times, flattening of the front face of polyimide 22 can be

carried out even to extent which irregularity can disregard mostly in a subsequent process. In the application than to which greater importance is not attached so much to surface irregularity, the above does not need to perform a flat chemically-modified degree. In addition, with the following operation gestalten, in order to simplify explanation, on a drawing, it explains as that to which the front face became flat altogether. By the above, the top face of the layer flow post 18 can form an interlayer insulation film (polyimide 22) in the form exposed certainly.

[0054] In order to form the circuit pattern 31 of a bilayer eye on a <bilayer eye circuit pattern formation process> interlayer insulation film (polyimide 22), the completely same much more process as an eye is performed. That is, each process of IPA washing, UV irradiation washing, the formation of ** ink by the alkyl fluoride silane, adjustment of the contact angle by UV irradiation, the pattern regurgitation of silver particle content ink, and hot air drying is performed. And only a required count repeats the process of regurgitation -> hot-air-drying -> regurgitation -> hot air drying.

[0055] After forming the layer flow post 32 like the 1st layer as shown in drawing 3 (a) in multilayering furthermore, it calginates to bilayer eye wiring and coincidence, and a flow is aimed at. The interlayer insulation film 33 for 2 or 3 layers as shown by drawing 3 (b) is formed completely like the time of forming the interlayer insulation film between 1 and two-layer (polyimide 22) from moreover. Such an any number-of layers process can be multilayered because only a required count repeats. Drawing 3 (c) is the example formed to the third layer.

[0056] (The 2nd operation gestalt) Drawing 4 is process drawing showing the manufacture approach of the multilayer-interconnection substrate concerning the 2nd operation gestalt of this invention. Multilayer printed wiring is formed in both sides of the core substrate 40 with this operation gestalt.

[0057] In having carried out the laminating of a circuit pattern and the insulator layer pattern, and having formed them by the drop regurgitation method, like the 1st operation gestalt, only the same single-sided board as the 1st operation gestalt is made. What is necessary is just to perform the same process as the 1st operation gestalt to both-sides side as a core substrate 40 which takes the lead using the usual double-sided wiring substrate by making this into a starting point, in order to form multilayer printed wiring in both sides of a substrate.

[0058] However, it is desirable to use the thing of the type which does not have a through hole as a core substrate 40, and this has the approach of filling up a through hole with the metal paste 41, the approach of making the non-through hole to copper foil in a single-sided copper foil substrate, and filling up into it with a metal paste, etc. The usual photolithography or laser radiation performs drilling. Moreover, the approach of filling up with a drop regurgitation method into a through hole or a non-through hole the conductive ink containing the same silver particle as what was used with the 1st operation gestalt may be used.

[0059] Thus, multilayer printed wiring can be formed in both sides of the core substrate 40 by leaving the condition that the circuit pattern was formed in core substrate 40 both sides, and repeating successively the process which forms the layer flow post 42, the process which forms an interlayer insulation film 43, and the process which forms the circuit pattern 44 of the following layer to both sides.

[0060] (The 3rd operation gestalt) Drawing 5 is process drawing showing the manufacture approach of the multilayer-interconnection substrate concerning the 3rd operation gestalt of this invention. This operation gestalt draws a circuit pattern suddenly, and forms multilayer printed wiring on what [what forms rewiring by the chip scale package (CSP:Chip Scale Package) technique], i.e., a chip.

[0061] First, as shown in drawing 5 (a), ** ink processing is carried out to the IC chip 50 which even the aluminum pad 51 formed using a monomolecular film. This processing is almost the same as the processing performed with the 1st operation gestalt, and is the same as ** ink processing of the 1st operation gestalt except having used decyltriethoxysilane as an ingredient of a monomolecular film.

[0062] Subsequently, as shown in drawing 5 (b), the layer with a diameter of 50 micrometers electric conduction post 52 is formed in the core of all the aluminum pads 51 in height of 5 micrometers according to the same process as the 1st operation gestalt. Furthermore, an interlayer insulation film 53

is formed according to the same process as the 1st operation gestalt to the same height as the top face of the layer electric conduction post 52. By this, the interlayer insulation film 53 with a flat front face can be formed, exposing certainly the top face of the layer electric conduction post 52.
[0063] Then, rewiring 54 is formed from the aluminum pad 51 of the IC chip 50 like drawing 5 (c) by performing the process of electric conduction pillar ** -> interlayer insulation film formation like the above between ** ink processing -> bilayer eye wiring layer formation -> layers. Subsequently, the bump 56 prepared on a pad 55 and its pad 55 is formed by the same approach as the wiring formation in a usual photolithography or the usual 1st operation gestalt after the layer electric conduction post 52 which has appeared in the substrate front face.
[0064] (The 4th operation gestalt) Drawing 6 is process drawing showing the manufacture approach of the multilayer-interconnection substrate concerning the 4th operation gestalt of this invention. This operation gestalt forms the coil configuration of the antenna trailer in wireless IC card 60 by the manufacture approach of the above-mentioned operation gestalt. In addition, drawing 6 (a'), drawing 6 (b'), and drawing 6 (c') show the sectional view between the two pad sections 65 in drawing 6 (a), drawing 6 (b), and drawing 6 (c), respectively.
[0065] This wireless IC card 60 consists of an IC chip 63 mounted in the polyimide film 61, and a coiled form antenna 62. The IC chip 63 consists of nonvolatile memory, a logical circuit, a RF circuit, etc., and it operates by catching the electric wave taken out from the external transmitter with an antenna 62, and receiving an electric power supply. Moreover, the IC chip 63 analyzes the signal which the antenna 62 received, and makes the required predetermined signal corresponding to the analysis result send from an antenna 62.
[0066] In order to create such a wireless IC card, as shown in drawing 6 (a), the coiled form antenna 62 is first formed on a polyimide film 61 like the 1st layer wiring formation process of the first operation gestalt. Terminal area 63a which mounts the pad section 64 and the IC chip 63 is also formed simultaneously with an antenna 62. After forming an antenna 62, the layer flow post 65 is further formed on the pad section 64 like the first operation gestalt. Subsequently, as shown in drawing 6 (b) like the 1st operation gestalt, polyimide is applied to a pattern and an interlayer insulation film 66 is formed so that the top face of the layer flow post 65 may come out.
[0067] After forming an interlayer insulation film 66, further, like the 1st operation gestalt, the conductive ink of silver particle content is applied to a pattern as shown in drawing 6 (c) by the drop regurgitation method, and the wiring 67 which calcinates and connects the ends of the coiled form antenna 62 after that is formed. Finally, the IC chip 63 is mounted in the location of drawing 6 (C) using an anisotropy electric conduction film, and the whole is laminated with the protection film which is not illustrated further, and it becomes wireless IC card 60. This wireless IC card 60 can communicate with the reader/writer of the exterior distant 5cm, for example.
[0068] In addition, when the pad section 64 is comparatively as large as several mm angle, even if it does not form the layer flow post 65, multilayer printed wiring can be prepared by leaving a field required for the flow between layers, and forming an interlayer insulation film 66. In this case, the part of the edge of the layer insulation layer 66 can form wiring 67 with a drop regurgitation method, without disconnecting on that layer insulation layer 66, since it becomes a configuration with a taper.
[0069] (Electronic equipment) The example of electronic equipment equipped with the substrate manufactured using the manufacture approach of the multilayer-interconnection substrate of the above-mentioned operation gestalt is explained. Drawing 7 is the perspective view having shown an example of a cellular phone. In drawing 7 , a sign 1000 shows the body of a cellular phone, and the sign 1001 shows the display using the multilayer-interconnection substrate manufactured by the manufacture approach of the above-mentioned operation gestalt.
[0070] Drawing 8 is the perspective view having shown an example of wrist watch mold electronic equipment. In drawing 8 , a sign 1100 shows the body of a clock and the sign 1101 shows the display using the multilayer-interconnection substrate manufactured by the manufacture approach of the

above-mentioned operation gestalt.
[0071] Drawing 9 is the perspective view having shown an example of pocket mold information processors, such as a word processor and a personal computer. In drawing 9 , as for the information processor and the sign 1202, the sign 1200 shows the display using the multilayer-interconnection substrate with which the input sections, such as a keyboard, and a sign 1204 were manufactured by the body of an information processor, and the sign 1206 was manufactured by the manufacture approach of the above-mentioned operation gestalt.
[0072] It can shorten a manufacture period while it is manufactured by the precision by the production process simpler than the conventional thing, since the electronic equipment shown in drawing 9 from drawing 7 is equipped with the multilayer-interconnection substrate manufactured by the manufacture approach of the above-mentioned operation gestalt.
[0073] In addition, the technical range of this invention is not limited to the above-mentioned operation gestalt, it cannot pass over a concrete ingredient, lamination, the manufacture approach which it is possible to add various modification in the range which does not deviate from the meaning of this invention, and were mentioned with the operation gestalt to a mere example, but they can be changed suitably. For example, the manufacture approach concerning this invention is not limited to manufacture of multilayer printed wiring, and can be applied to multilayer interconnections, such as a large-sized display unit.
[0074]
[Effect of the Invention] according to [so that clearly / in the above explanation] this invention -- a conductor -- since a drop regurgitation method is used and an interlayer insulation film is prepared around a post, it becomes possible to form an elaborate multilayer interconnection by the comparatively simple production process.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is process drawing showing the manufacture approach of the multilayer-interconnection substrate concerning the 1st operation gestalt of this invention.
[Drawing 2] It is process drawing showing the manufacture approach of the multilayer-interconnection substrate concerning the 1st operation gestalt of this invention.
[Drawing 3] It is process drawing showing the manufacture approach of the multilayer-interconnection substrate concerning the 1st operation gestalt of this invention.
[Drawing 4] It is process drawing showing the manufacture approach of the multilayer-interconnection substrate concerning the 2nd operation gestalt of this invention.
[Drawing 5] It is process drawing showing the manufacture approach of the multilayer-interconnection

substrate concerning the 3rd operation gestalt of this invention.
[Drawing 6] It is process drawing showing the manufacture approach of the multilayer-interconnection substrate concerning the 4th operation gestalt of this invention.
[Drawing 7] It is drawing showing an example of electronic equipment equipped with the electro-optic device of this operation gestalt.
[Drawing 8] It is drawing showing an example of electronic equipment equipped with the electro-optic device of this operation gestalt.
[Drawing 9] It is drawing showing an example of electronic equipment equipped with the electro-optic device of this operation gestalt.
[Description of Notations]
10 Substrate
11 Ink Jet Head
12, 13, 15 Drop
14 Ink Droplet
16 Pattern
17 Circuit Pattern
18 Layer Flow Post (Conductor Post)
21 Ink
22 Polyimide (Interlayer Insulation Film)
31 Circuit Pattern (Bilayer Eye)
32 Layer Flow Post
33 Interlayer Insulation Film
40 Core Substrate
41 Metal Paste
42 Layer Flow Post
43 Interlayer Insulation Film
44 Circuit Pattern
50 IC Chip
51 Aluminum Pad
52 Layer Electric Connection Post
53 Interlayer Insulation Film
54 Rewiring
55 Pad
56 Bump
60 Wireless IC Card
61 Polyimide Film
62 Antenna
63 IC Chip
63a The connection of IC chip
64 Pad Section
65 Layer Flow Post
66 Interlayer Insulation Film
67 Wiring

[Translation done.]